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ABSTRACT OF THE DISCLOSURE

A timing control method for operating a synchronous memory. The synchronous memory has a local data bus, a signal amplification bus and a global data bus. The timing control method includes manipulating the local data bus, the signal amplification bus and the global bus such that a series of operations including pre-charging the local data buses, developing signals on the amplifier buses is performed
10 evenly within one clock cycle. Amplifying and transferring local data to global data is moved to next cycle and hid within the local data pre-charging period.